

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Form PTO-1449 (Modified) (Use several sheets if necessary)				COMPLETE IF KNOWN	
				Application Number:	10/612,840
				Art Unit No.:	2631
				Filing Date:	July 3, 2003
				First Named Inventors:	Yongsam Moon et al.
				Examiner:	To be assigned
Sheet	1	of	2	Attorney Docket No.	59472-8086.US03

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No.	U.S. Patent or Application		Name of Patentee or Inventor of Cited Document	Date of Publication or Filing Date of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		NUMBER	Kind Code (if known)			

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No.	Foreign Patent or Application			Name of Patentee or Applicant of Cited Document	Date of Publication or Filing Date of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
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OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume issue number(s), publisher, city and/or country where published.	T
LW	A	Lee, C. Yoo, W. Kim, S. Chai, and W. Song, "A 622Mb/s CMOS Clock Recovery PLL with Time-Interleaved Phas Detector Array," in <i>IEEE ISSCC Dig. Tech. Papers</i> , Feb. 1996, pp. 198-199.	
LW	B	Fiedler, R. Mactaggart, J. Welch, and S. Krishnan, "A 1.0625 Gbps Transceiver with 2x-Oversampling and Transmit Signal Pre-Emphasis," in <i>IEEE ISSC Dig. Tech. Papers</i> , Feb. 1997, pp. 238-239.	
LW	C	R. Gu, J. M. Tran, H.-C. Lin, A.-L. Yee, and M. Izzard, "A 0.5 – 3.5Gb/s Low-Power Low-Jitter Serial Data CMOS Transceiver," in <i>IEEE ISSCC Dig. Tech. Papers</i> , Feb. 1999, pp. 352-353.	
LW	D	T. H. Lee, K. S. Donnelly, J. T. C. Ho, J. Zerbe, M. G. Johnson, and T. Ishikawa, "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM," <i>IEEE J. Solid-State Circuits</i> , Vol. 29 (12/1994), pp. 1491-1496.	
LW	E	Efendovich, Y. Afek, C. Sella, and Z Bikowsky, "Multifrequency Zero-Jitter Delay-Locked Loop," <i>IEEE J. Solid-State Circuits</i> , Vol. 29, No. 1 (1/1994), pp. 26-70.	

EXAMINER /Lawrence Williams/ (11/16/2006)	DATE CONSIDERED
*EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to application(s).	

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Sheet 2 of 2 Attorney Docket No. 59472-8086.US03

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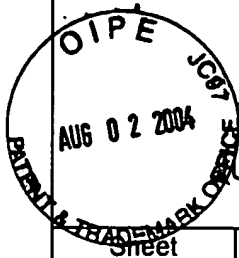
OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS

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LW	F	S. Sidiropoulos, and M. A. Horowitz, "A Semi-Digital Dual Delay-Locked Loop," <i>IEEE J. Solid-State Circuits</i> , Vol. 32, No. 11, (11/1997), pp. 1683-1692.	
LW	G	Y. Moon, J. Choi, K. Lee, D.-K. Jeong, and M.-K Kim, "An All-Analog Multiphase Delay-Locked Loop Using a Replica Delay Line for Wide-Range Operation and Low-Jitter Performance," <i>IEEE J. Solid-State circuits</i> , Vol. 35, (3/2000), pp. 377-384.	
LW	H	Ian A. Young, J. K. Greason, and K. L. Wong, "A PLL Clock generator with 5 to 100 MHz of Lock Range for Microprocessors", <i>IEEE Journal of Solid-State Circuits</i> , Vol. SC-27, (11/1992), pp. 1599-1607.	

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/Lawrence Williams/ (11/16/2006)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

Form PTO-1449 (Modified)
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COMPLETE IF KNOWN

Application Number	10/612,840
Confirmation Number	6861
Filing Date	July 3, 2003
First Named Inventor	Yongsam Moon
Group Art Unit	2631
Examiner Name	Not Assigned
Attorney Docket No.	59472-8086.US03

Sheet 1 of 1

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LW		6,437,619		Okuda et al.	08/2002	
LW		6,442,225		Huang	06/14/99	
LW		6,667,643		Ko, Myeong-lyong	12/2003	
LW		6,683,930		Dalmia	12/23/99	
LW		6,700,944		Chlipala et al.	05/30/00	

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OCT 18 2004

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**SUPPLEMENTAL INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
Form PTO-1449 (Modified)
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Application Number 10/612,840
Confirmation Number 6861
Filing Date July 3, 2003
First Named Inventor Yongsam Moon
Group Art Unit 2631
Examiner Name Not Assigned
Attorney Docket No. 59472-8086.US03

Sheet 1 of 1

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LW		4,773,085		Cordell	09/20/88	
LW		4,594,564		Yarborough	06/10/86	
LW		4,970,581		O'Gwynn	11/13/90	
LW		5,966,030		Schmitt, et al.	10/12/00	

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